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VO, TUNG T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/672,195	Applicant(s) MARTEMYANOV ET AL.	
	Examiner Tung Vo	Art Unit 2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 14 June 2007.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-4,6-31 and 33-37 is/are pending in the application.

4a) Of the above claim(s) 5 and 32 is/are withdrawn from consideration.

5)☒ Claim(s) 13-31 and 33-37 is/are allowed.

6)☒ Claim(s) 1-4 and 6-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 7-8, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sethuraman et al (US 6,434,196) in view of Takahashi et al. (US 6,683,992).

Re claim 1. Sethuraman teaches a video codec (fig. 1) for encoding/decoding digitized sequence of video frames with high compression efficiency, comprising:

a frame encoder (100 of fig. 1) for frame encoding receiving video frame pixels (101 of fig. 1) and providing coded bitstream and reconstructed frame structure (125 and 130 of fig. 1);

a codec setting unit (140 of fig. 1) for setting and storing codec setting parameters;

a CPU load controller (140-4 of fig. 1) for controlling desired frame encoding time (Note The microprocessor 140-4 cooperates with conventional support circuitry 140-6 such as power supplies, clock circuits, cache memory and the like as well as circuits that assist in executing the software methods, so this would obviously suggest the desired frame encoding time and CPU loading); rate controller (200 of fig. 1) for controlling size of the frame encoding encoder output bitstream; and

a transform encoder (110, 115, and 120 of fig. 1) for arithmetic coding of quantized transform coefficients; and

a noise suppression unit (101 and 150 of fig. 1) for suppressing noise level by applying a block motion estimate (151 and 152 of fig. 1) for every block of each pair of two successive frames; comparing intensities of pixels in the same position in corresponding blocks of a first frame and a second frame of each pair (Full pel motion estimation, 151 of fig. 1), and, if an absolute difference between said intensities does not exceed a predetermined noise suppression level (415-1 of fig. 4, Note the motion estimation does not exceed to the predetermined noise, so using half pixel motion estimation is used), replacing the intensity of the pixel in the second frame by a half-sum of said intensities (415-2 of fig. 4); a memory unit for storing reference frames (170 of fig. 1); means for motion compensation to perform motion estimation, frame head coding, macroblock encoding and coded frame reconstruction and storage (145 of fig. 1); an intra prediction unit and at least one inter prediction unit (105 of fig. 1), a macroblock setting unit for selecting macroblock type (170 of fig. 1) and encoding setting; a vector calculator for calculating motion vector prediction and prediction error (150 and 145 of fig. 1).

It is noted that Sethuraman does not particularly teach a calculator for calculating macroblock texture prediction and prediction error, means a quantization unit for performing texture prediction error transform and transform coefficient quantization; and an entropy encoding unit for providing arithmetic context encoding of motion vectors, header parameters and transform coefficients; decoding means performing arithmetic context-based decoding using decoding modeling corresponding to arithmetic encoding of the codec; the decoding means comprises means for motion vector reconstruction, transform coefficient inverse quantization, texture prediction inverse transform, and reconstructed macroblock texture unit.

Takahashi teaches (figs 8 and 11) a calculator (1101-1110 and 1201-1202 of fig. 11) for calculating macroblock texture prediction and prediction error, means a quantization unit (1104 of fig. 11) for performing texture prediction error transform and transform coefficient quantization; and an entropy encoding unit (1001 of fig. 1) for providing arithmetic context encoding of motion vectors (12a of fig. 8), header parameters and transform coefficients; decoding means performing arithmetic context-based decoding using decoding modeling corresponding to arithmetic encoding of the codec; the decoding means (802a of fig. 8) comprises means for motion vector reconstruction, transform coefficient inverse quantization, texture prediction inverse transform, and reconstructed macroblock texture unit (1105, 1106, 1108 of fig. 11, Note elements are used for decoder).

Therefore, taking the teachings of Sethuraman and Takahashi as a whole it would have obvious to one of ordinary skill in the art to incorporate the arithmetic encoding and decoding of Takahashi into the system of Sethuraman for the decoding LSI can perform high-speed decoding on a bitstream corresponding to plural objects, such as images, which are compressively coded by the MPEG4 coding method, with reduced cost of the hardware circuits performing the decoding process.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable Sethuraman et al (US 6,434,196) in view of Takahashi et al. (US 6,683,992) as applied to claim 1, and further in view of Lee et al. (US 6,81,554).

Re claim 3, the combination of Sethuraman and Takahashi does not particularly teach mean for downscaling before encoding of the video frame using bilinear interpolation and up scaling correlated with bilinear downscaling provided at the time of encoding as claimed.

However, Lee teaches means for downscaling (220 of fig. 2; Down sampling) before encoding of the video frame using bilinear interpolation (fig. 3); and bilinear up scaling (230 of fig. 2, Up sampling) correlated with bilinear downscaling provided at the time of encoding. Lee further suggests various modifications and alterations to the described embodiments will be apparent to those skilled in the art in view of the teachings herein (col. 12,lines 44-49).

Therefore, taking the teachings of Sethuraman, Takahashi, and Lee as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Lee into the combined video codec of Sethuraman and Takahashi for providing capability to any video compression process requiring the minimization of distortion under buffer constraints that would reduce buffer occupancy.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sethuraman et al (US 6,434,196) in view of Takahashi et al. (Us 6,683,992) as applied to claim 1, and further in view of Srinivasan (US 7,110,459).

Re claim 4, The combination of Sethuraman and Takahashi does not particularly teach deblocking means for processing reconstructed frame texture to eliminate blocking effect restored data encoded at high distortion and noise suppression as claimed.

However, Srinivasan teaches deblocking means for processing reconstructed frame texture to eliminate blocking effect restored data encoded at high distortion and noise suppression (col. 10, lines 9-11).

Therefore, taking the teachings of Sethuraman, Takahashi, and Srinivasan as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Srinivasan into the combined video codec of Sethuraman and Takahashi to provide a video encoder and decoder use one or more approximate bicubic filters when computing pixel values at sub-pixel positions in reference video frames. This improves the effectiveness of motion prediction using the computed pixel values.

5. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sethuraman et al (US 6,434,196) in view of Takahashi et al. (US 6,683,992) as applied to claims 1 and 10, and further in view of Forchheimer et al..(US 6,594,395).

Re claims 9 and 11, the combination of Sethuraman and Takahashi does not particularly three-dimensional (3-D) frame encoding/decoding; means for selecting a codec mode between motion compensation and 3-D encoding/decoding, depending on desired reconstructed sequence quality and bitrate parameters; means for 3-D inverse transform and dequantization as claimed.

However, Forchheimer teaches three-dimensional (3-D) frame encoding/decoding (col. 2, lines 45-47; 3-D coding data, col. 6, lines 12-53); means for selecting a codec mode between motion compensation and 3-D encoding/decoding (col. 6, lines 12-53), depending on desired reconstructed sequence quality and bitrate parameters; means for 3-D inverse transform and

dequantization (SPTIAL DECODER of fig. 4, where IDCT and DQ are obviously implemented in the decoder (see fig. 8 of Maeda)).

Therefore, taking the teachings of Sethuraman, Takahashi, and Forchheimer as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Forchheimer into the combined video codec of Sethuraman and Takahashi in order to performing high compression efficiency to achieve video communication with low power terminals.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sethuraman et al (US 6,434,196) in view of Takahashi et al. (US 6,683,992) and further in view of Li et al. (US

Re claim 1. Sethuraman teaches a video codec (fig. 1) for encoding/decoding digitized sequence of video frames with high compression efficiency, comprising:

a frame encoder (100 of fig. 1) for frame encoding receiving video frame pixels (101 of fig. 1) and providing coded bitstream and reconstructed frame structure (125 and 130 of fig. 1);

a codec setting unit (140 of fig. 1) for setting and storing codec setting parameters;

a CPU load controller (140-4 of fig. 1) for controlling desired frame encoding time (Note The microprocessor 140-4 cooperates with conventional support circuitry 140-6 such as power supplies, clock circuits, cache memory and the like as well as circuits that assist in executing the software methods, so this would obviously suggest the desired frame encoding time and CPU loading);

a rate controller (200 of fig. 1) for controlling size of the frame encoding encoder output bitstream; and

a coding statistics memory (140-8 of fig. 1) for coding of bitstream parameters.

It is noted that Sethuraman does not particularly teach arithmetic encoding and decoding as claimed.

However, Takahashi a arithmetic encoding and decoding circuit (fig. 8) for encoding and decoding video context, texture, and shape of bitstream.

Therefore, taking the teachings of Sethuraman and Takahashi as a whole it would have obvious to one of ordinary skill in the art to incorporate the arithmetic encoding and decoding of Takahashi into the system of Sethuraman for the decoding LSI can perform high-speed decoding on a bitstream corresponding to plural objects, such as images, which are compressively coded by the MPEG4 coding method, with reduced cost of the hardware circuits performing the decoding process.

The combination of Sethuraman and Takahashi does not particularly teach means for an encoder for three-dimensional (3-D) frame encoding/decoding; wherein the 3D coding is provided by dividing the sequence of video frames into 3D frames, dividing each 3D frame into 3D macroblocks with a time as a third coordinate; transforming each 3D block into frequency domain with a 3D-DCT transform or combined DCT/wavelet transform, with coefficients of said transform coded as a texture difference blocks, with different arithmetic models used for different temporal frequency layers as claimed.

However, Li teaches means for an encoder for three-dimensional (3-D) frame encoding/decoding; wherein the 3D coding is provided by dividing the sequence of video frames into 3D frames (fig. 4), dividing each 3D frame into 3D macroblocks with a time as a third coordinate; transforming each 3D block into frequency domain with a 3D-DCT transform or

combined DCT/wavelet transform (130 of fig. 4), with coefficients of said transform coded as a texture difference blocks (134 of fig. 4), with different arithmetic models used for different temporal frequency layers (figs. 3-5).

Therefore, taking the teachings of Sethuraman, Takahashi, and Li as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Li into the combined codec of Sethuraman and Takahashi for more efficiently compressing/decompressing object-based data in a video bitstream.

Allowable Subject Matter

7. Claims 13-31 and 33-37 are allowed.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung Vo whose telephone number is 571-272-7340. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tung Vo
Primary Examiner
Art Unit 2621